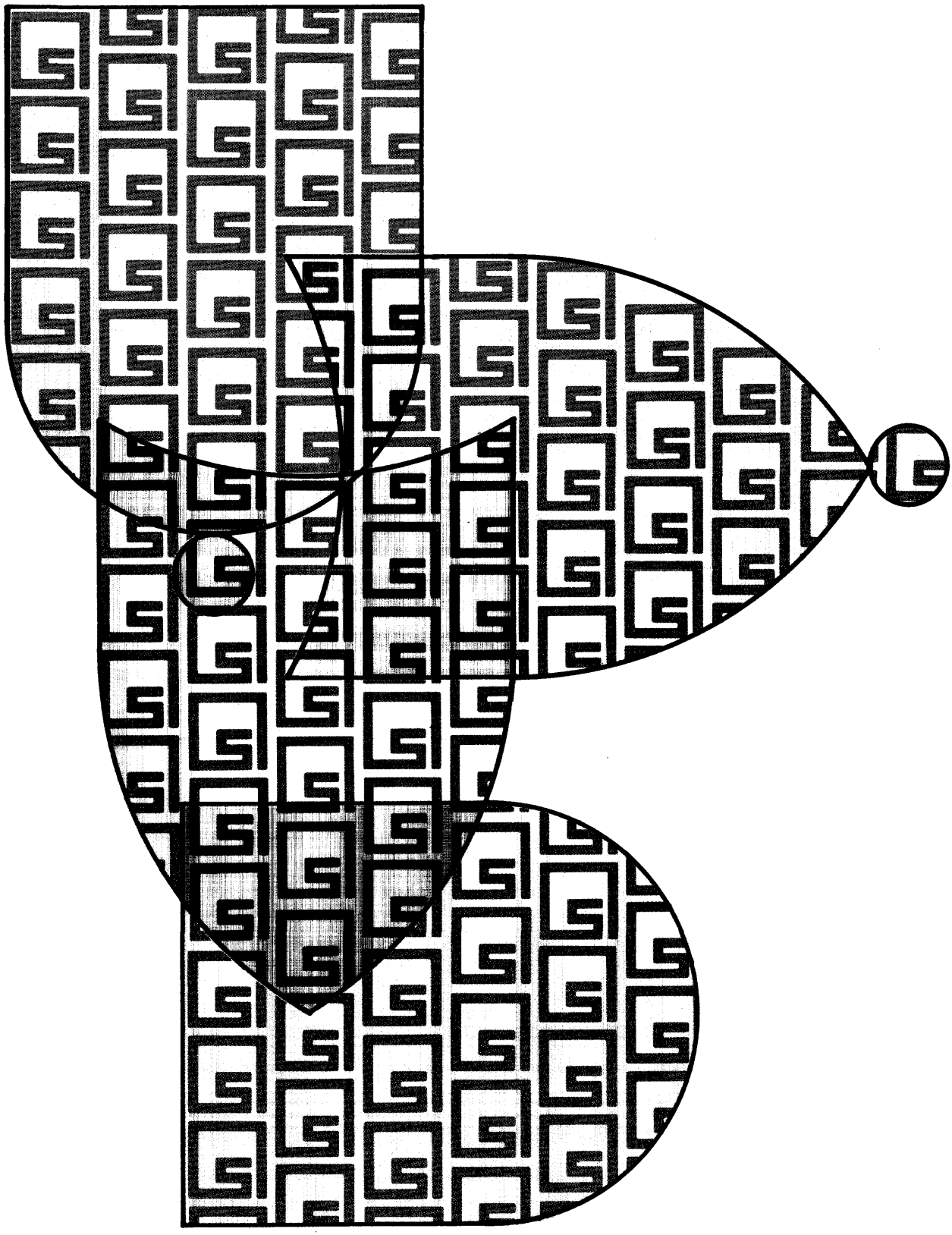
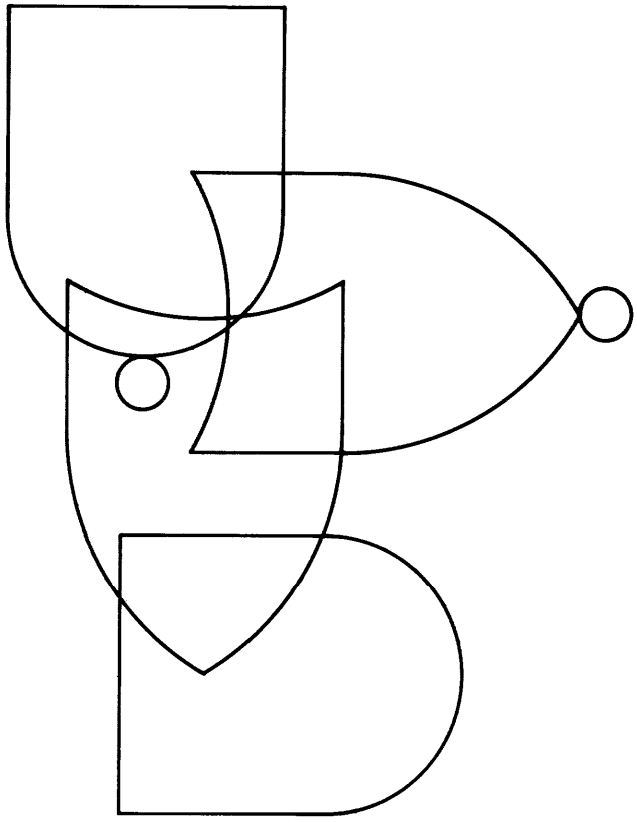


SIGNETICS UTILOGIC II HANDBOOK



UTILOGIC II HANDBOOK

TABLE OF CONTENTS

TABLE OF CONTENTS Continued

UTILOGIC II

SP300A SERIES (0°C to +75°C)

LU300A SERIES (+10°C to +55°C)

DUAL IN-LINE PACKAGING
GREATER THAN 1-VOLT DC NOISE MARGINS

UTILOGIC II is a newly engineered version of Signetics original UTILOGIC family which was introduced in 1964. New devices and features in UTILOGIC II include dual in-line plug-in package, two new dual J-K binaries, a complete complement of OR, NOR, AND, and NAND gates, as well as a dual buffer and a one shot.

The proven performance of the earlier UTILOGIC family, including greater than 1 volt noise margins and high capacitive drive capability has been retained. The simplicity of the Signetics silicone package provides inherently low cost in both manufacturing and subsequent handling by the user. The reliability of the Signetics silicone package has been proved by over three years of exhaustive testing. A copy of the Signetics package reliability report is available on request.

UTILOGIC II elements are available in two temperature ranges: those with SP prefixes are for applications in the 0°C to 75°C range, and those with LU prefixes in the +10°C to +55°C range.

The suffix A signifies the 14-pin dual in-line package; the suffix B signifies the 16-pin dual in-line package.

At the time of the writing of this handbook (March 1969), the UTILOGIC II family consists of the following elements:

NOR Gates

314A	Single 7-Input NOR Gate
317A	Dual 4-Input Expandable NOR Gate
370A	Triple 3-Input NOR Gate
380A	Quad 2-Input NOR Gate

OR Gates

333A	Dual 3-Input Expandable OR Gate
334A	Dual 4-Input Expandable OR Gate
374A	Triple 3-Input OR Gate
375A	Triple 2-Input Expandable OR Gate
384A	Quad 2-Input OR Gate

AND Gates

305A	Single 6-Input AND Gate
306A	Dual 3-Input AND Gate

NAND Gates

337A	Dual 4-Input Expandable NAND Gate
377A	Triple 3-Input NAND Gate
387A	Quad 2-Input NAND Gate

Gate Expanders

300A	Dual 3-Input Expander for OR and NOR Gates
301A	Quad 2-Input Diode Expander for NAND Gates

Line Drivers

356A	Dual 4-Input Expandable NAND Line Driver

Binaries

321A	Dual J-K Binary
322B	Dual J-K Binary

Multivibrator

362A	Monostable Multivibrator

LOADING DEFINITIONS

UTILOGIC II loads are classified as "sink loads," or current out of the load inputs, and as "source loads," or current into the load inputs. The standard sink load is the input of a UTILOGIC II AND gate. The standard source load is the input of a UTILOGIC II NOR gate. See loading chart for specific values.

NOISE MARGINS

Signetics specifies noise immunity on UTILOGIC II NOR gates in terms of DC margins determined under worst conditions for both the "0" and "1" levels. The margin for a "1" input applies to negative-going noise on the high level or on the power supply line. The margin for a "0" input applies to positive-going noise on the low logic level or the ground line.

The DC margin is defined as the difference between the worst case output level and the worst case input threshold. Output levels for the NOR are 3.8 volts or greater for the "1" level and 0.6 volts or less for the "0" level. The corresponding input thresholds are 2.7 volts for "1" and 1.4 volts for "0". Thus, the minimum DC margins are specified as 1100 mV for "1" and 800 mV for "0" levels.

Current margins, which Signetics specifies in addition to the familiar voltage margins, are quite useful to the designer because current margins provide a measure of the amount of coupling necessary to cause an erroneous output. Specifications state that the UTILOGIC II NOR's can supply 2 mA at the "1" level and sink 12.5 mA at the "0" level. The maximum specified fan-out of these elements is 11 source loads (requiring 1.98 mA) and 5 sink loads (requiring 12.5 mA).

For AND gates, maximum offset voltages, which are more appropriate to non-saturating gates, are specified. These offset voltages ensure maintenance of high DC margins in cascaded logic configurations.

OPERATING VOLTAGE FOR ALL UTILOGIC II ELEMENTS: 5V ±5%

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

VOLTAGE APPLIED (All Terminals)	±5.5V (Note 4)
CURRENT RATING (All Input Terminals)	±10 mA (Note 4)
CURRENT RATING (All Other Terminals)	±50 mA (Note 4)
OPERATING TEMPERATURE (SP300)	0°C to +75°C
OPERATING TEMPERATURE (LU300)	+10°C to +55°C

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 – Standard Conditions: V_{CC} = +5.0V, T = +25°C)

300 EXPANDER

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
EXPANSION FORWARD VOLTAGE	V_{OUT}	1.85			V	V_{IN} = +2.7V, R_{OUT} = 590Ω ±1% to 0V
AVERAGE GATE DELAY	t_{pd}		5.0		ns	Measured at 50% points
FAN-IN EXPANSION OF 317				33		See text under "NOR GATES"

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 5 – Standard Conditions: V_{CC} = +5.0V, T = +25°C)

301 EXPANDER

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" INPUT CURRENT	I_{in}			10	μA	+75°C, V_{in}:5.0V
DIODE FORWARD VOLTAGE	V_{in}			0.9	V	$I_{FORWARD}$ 2.5mA

314, 317, 370 and 380 NOR GATES

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		800	1200		mV	Note 8
NOISE IMMUNITY FOR "1"		1100	1700		mV	Note 8
"1" OUTPUT VOLTAGE	V_{OUT}	3.8			V	I_{OUT} = –2 mA, V_{IN} = +1.4V
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA, V_{IN} = +2.7V
"1" INPUT CURRENT	I_{IN}			180	μA	V_{IN} = +2.7V
EXPANDER NODE VOLTAGE	V_N	1.85			V	V_{IN} = +2.7V
AVERAGE POWER CONSUMPTION			22		mW	Each gate; 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		20		ns	7-stage ring oscillator
	t_{pd}		30		ns	7-stage ring oscillator, C_L = 130 pF/gate
AVERAGE GATE DELAY	t_d		20		ns	Full Fan-out C_L = 8 pF to Gnd;
	t_d		35		ns	Full Fan-out C_L = 130 pF to Gnd;
FAN-OUT						
To sink loads				5		Note 6, 7
To source loads				11		Note 6, 7

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 — Standard Conditions: V_{CC} = +5.0V, T = +25°C)

356 LINE DRIVER

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"			800		mV	Note 8
NOISE IMMUNITY FOR "1"			1500		mV	Note 8
"1" OUTPUT VOLTAGE	V_{OUT}	3.5			V	I_{OUT} = −2 mA, V_{IN} = +1.0V
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 44 mA, V_{IN} = +2.7V
"0" INPUT CURRENT	I_{IN}			−2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			37		mW	Each gate, 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		55		ns	
FAN-OUT						
To sink loads				17		Note 6, 7
To source loads				11		Note 6, 7

337, 377, 387 NAND GATES

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		400	600		mV	Note 8
NOISE IMMUNITY FOR "1"		800	1200		mV	Note 8
"0" OUTPUT VOLTAGE	V_{out}		0.4	0.6	V	I_{out} = 30mA, V_{in} = 2.7V
			0.3	0.4	V	I_{out} = 12.5mA, V_{in} = 2.1V
"1" OUTPUT VOLTAGE	V_{out}	3.5			V	I_{out} = −1.08mA, V_{in} = 1.0V
"0" INPUT CURRENT	I_{in}	−0.5		−2.5	mA	V_{in} = 0.4V
EXPANDER INPUT CURRENT	I_{in}	−0.5		−2.75	mA	V_{in} = 0.9V
POWER DISSIPATION			35	45	mW	Per gate, 50% duty cycle
PROPAGATION DELAY	t_{pd}		45		ns	Full fan-out; C_L = 22 pF
FAN-OUT						
to Sink Loads				12		Note 6, 7
to Source Loads				6		Note 6, 7

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 — Standard Conditions: V_{CC} = +5.0V, T = +25°C)

321, 322 DUAL J-K BINARIES

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" OUTPUT VOLTAGE	V_{OUT}	3.8			V	I_{OUT} = −1.6 mA
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA
"0" INPUT CURRENT: CLOCK, S_D, R_D INPUTS						
(321) CLOCK, R_D	I_{IN}			−6.2	mA	V_{IN} = 0.6V
(322) CLOCK, R_D	I_{IN}			−3.1	mA	V_{IN} = 0.6V
(321, 322) S_D	I_{IN}			−3.1	mA	V_{IN} = 0.6V
(321, 322) J-K	I_{IN}			−1.6	mA	V_{IN} = 0.6V
"1" INPUT CURRENT (321, 322) J-K	I_{IN}			50*	μA	V_{IN} = 4.5V
AVERAGE POWER CONSUMPTION			90		mW	Each binary
AVERAGE PROPAGATION DELAY	t_{pd}		25		ns	Full Fan-out C_L = 50 pF, P.W. = 200 ns
AVERAGE PROPAGATION DELAY	t_{pd}		35		ns	Full Fan-Out C_L = 130 pF, P.W. = 200 ns
FAN-OUT						
To sink loads				5		Notes 6, 7
To source loads				8		Notes 6, 7

*Proportionally higher on Clock, R_D and S_D inputs.

305, 306 AND GATES

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$			0.15	V	I_{OUT} = −1.8 mA, V_{IN} = +3.8V
"0" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$			−0.3	V	V_{IN} = +0.6V
"0" INPUT CURRENT	I_{IN}			−2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			6.0		mW	Each gate; 50% duty cycle
AVERAGE GATE DELAY (Measured at 50% points)	t_{pd}		15		ns	Full Fan-out C_L = 8 pF to Gnd;
	t_{pd}		35		ns	Full Fan-out C_L = 75 pF to Gnd;
FAN-OUT (To source loads)				10		Note 6

ELECTRICAL CHARACTERISTICS (Notes1,2,5 – Standard Conditions: V_{cc} = +5.0V, T = +25°C)

333, 334, 374, 375, 384 OR GATES

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		800	1200		mV	Note 8
NOISE IMMUNITY FOR "1"		1100	1700		mV	Note 8
"1" OUTPUT VOLTAGE	V_{out}	3.8			V	I_{out} = -2mA, V_{in} = +2.7V
"0" OUTPUT VOLTAGE	V_{out}			0.6	V	I_{out} = 12.5mA, V_{in} = +1.4V
"1" INPUT CURRENT	I_{in}			180	μA	V_{in} = +2.7V
EXPANDER NODE VOLTAGE	V_n	1.85			V	V_{in} = +2.7V
AVERAGE POWER CONSUMPTION			44		mW	Each gate; 50% duty cycle
AVERAGE GATE DELAY	t_d		35		ns	R_L = 1.6K to Gnd; C_L = 130pF to Gnd; F.O. = 12
FAN-OUT						
To sink loads				5		Note 6, 7
To source loads				11		Note 6, 7

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 5, 9 – Standard Conditions: V_{cc} = 5.0V, T_A = +25°C, R_x = V_{cc})

362 MONOSTABLE MULTIVIBRATOR

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		800	1000		mV	Note 8
NOISE IMMUNITY FOR "1"		800	1200		mV	Note 8
"0" OUTPUT VOLTAGE	V_{out}		0.4	0.6	V	I_{out} = 12.5mA (Y and $\overline{Y}$)
	V_{out}		0.3	0.4	V	I_{out} = 7.5mA (Y and $\overline{Y}$)
"1" OUTPUT VOLTAGE	V_{out}	3.5			V	I_{out} = 360μA (Y and $\overline{Y}$)
TRIGGER INPUT "1" CURRENT	I_{in}			10	μA	V_{in} = 5.0V

362 (Cont)

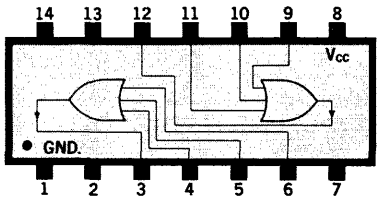
ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 5, 9 – Standard Conditions: V_{cc} = 5.0V, T_A = +25°C, R_X = V_{cc})

CHARACTERISTIC	MEASURE-MENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TURN OFF DELAY	t_{off}		45		ns	Y, I_{out} = 360μA
TURN ON DELAY	t_{on}		35		ns	$\overline{Y}$, I_{out} = 12.5mA
OUTPUT FALL TIME	t_f		40		ns	$\overline{Y}$, C_L = 150pF
OUTPUT PULSE WIDTH	PW		50		ns	Y and $\overline{Y}$, I_{out} = 12.5mA
POWER DISSIPATION	P_O			125	mW	
FAN-OUT						
To sink loads				5		Note 6, 7
To source loads				2		Note 6, 7

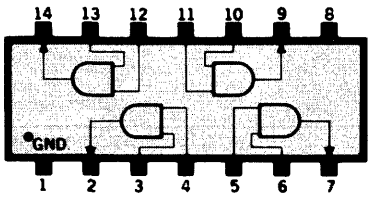
NOTES:

1. Pins not specifically referenced are left electrically open.
2. All voltage measurements are referenced to the ground pin.
3. Positive current flow is defined as into the terminal indicated.
3. Maximum ratings are values above which serviceability may be impaired.
4. Precautionary measures should be taken to ensure current limiting per the maximum ratings should the isolation diodes become forward biased.
5. Positive Logic Definition: "UP" Level = "1"; "DOWN" Level = "0".
6. Sink load is defined as a 306 input, source load is defined as a 317 input.
7. This device is capable of accommodating the maximum specified sink and source loads concurrently.
8. This characteristic guaranteed by output voltage measurements.
9. Manufacturer reserves right to make design and process improvements.

EXPANDERS

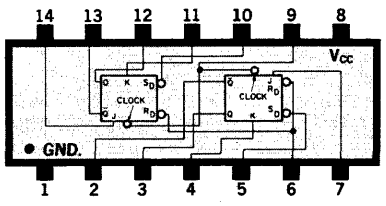


300A
DUAL 3-INPUT EXPANDER

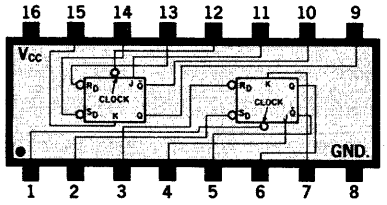


301A
QUAD 2-INPUT GATE EXPANDER

BINARIES

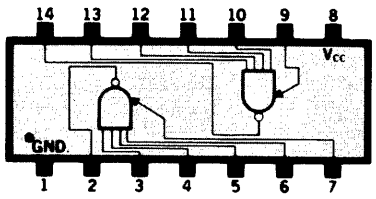


321A
DUAL J-K BINARY

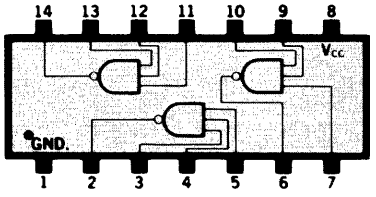


322B
DUAL J-K BINARY

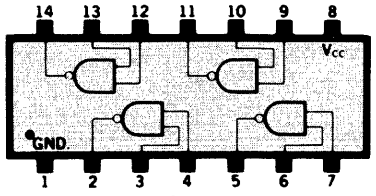
NAND GATES



337A
DUAL 4-INPUT EXPANDABLE NAND GATE

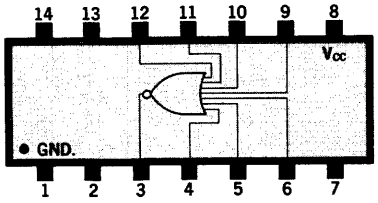


377A
TRIPLE 3-INPUT NAND GATE

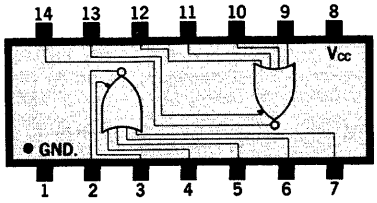


387A
QUAD 2-INPUT NAND GATE

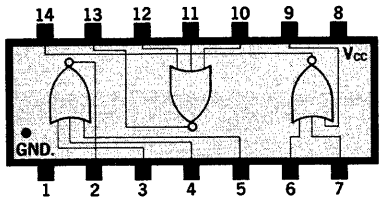
NOR GATES



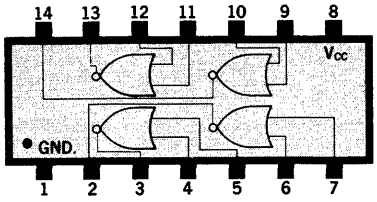
314A
7-INPUT NOR GATE



317A
DUAL 4-INPUT EXPANDABLE NOR GATE

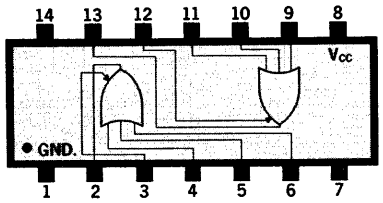


370A
TRIPLE 3-INPUT NOR GATE

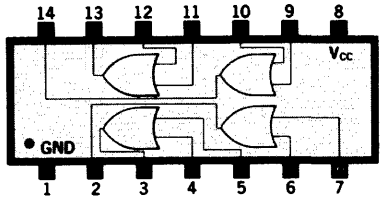


380A
QUAD 2-INPUT NOR GATE

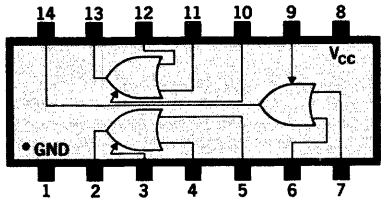
OR GATES



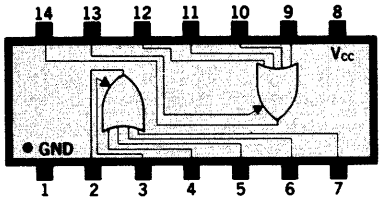
333A
DUAL 3-INPUT EXPANDABLE OR GATE

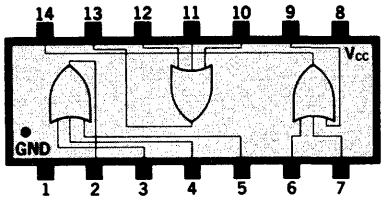


384A
QUAD 2-INPUT OR GATE



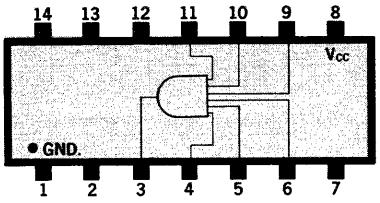
375A
TRIPLE 2-INPUT EXPANDABLE OR GATE



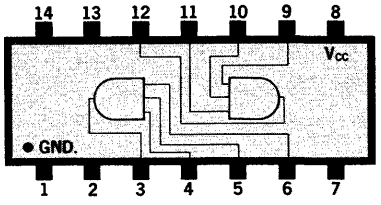


334A
DUAL 4-INPUT EXPANDABLE OR GATE

AND GATES

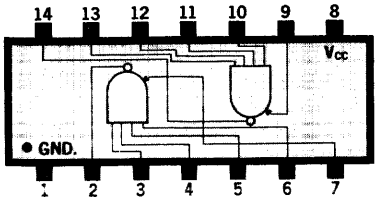


305A
6-INPUT AND GATE



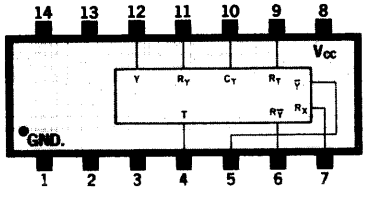
306A
DUAL 3-INPUT AND GATE

LINE DRIVER



356A
DUAL 4-INPUT EXPANDABLE LINE DRIVER

MONOSTABLE MULTIVIBRATOR



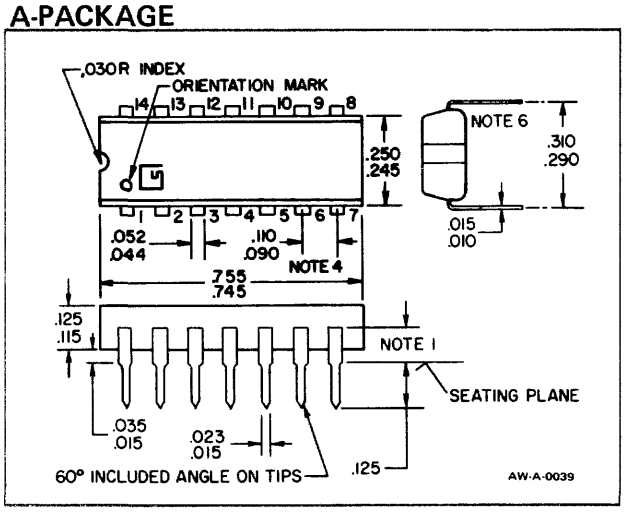
362 A
MONOSTABLE MULTIVIBRATOR

RELIABILITY OF SIGNETICS "A" and "B" PACKAGES

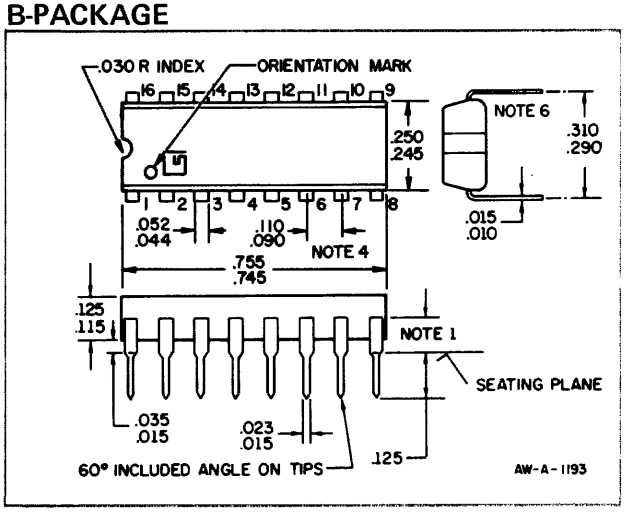
The Signetics solid molded package is capable of meeting or exceeding all of the moisture resistance requirements specified in MIL-S-19500 and MIL-STD-750. Furthermore, it meets or exceeds all other key mechanical, environmental and life test requirements of those specifications.

TEST	CONDITIONS
Solderability	All terminals
Temperature Cycling	10 Cycles, T = +125°C
Thermal Shock	5 cycles, 1 minute at each extreme, 0°C and +100°C, transfer time = 5 sec max
Moisture Resistance	Polarized and non-polarized
Shock	1500g; 5 blows y_1; 0.5 msec
Vibration, Fatigue	30g; non-operating
Vibration, Variable Frequency	30g
Acceleration	30,000g; 1 min. y_1
Operating Life	1000 hours at T_{min} = +85°C, dynamic operation at 100 kHz
Storage Life	1000 hours at T_{min} = +125°C

A-PACKAGE



B-PACKAGE



NOTES:
1. Lead spacing shall be measured within this zone.
2. Molded Plastic Body.
3. Kovar Leads.
4. Lead spacing tolerances are non-cumulative.
5. Thermal resistance from junction to still air, $\Theta_{J\text{-}A}$ = 0.16°C/mW.
6. Leads shown as positioned by Signetics dual in-line package carrier.
7. All dimensions of plastic package exclude molding-caused flash.

FAN-OUT

UTILOGIC II LOADING CHARTS

DRIVEN ELEMENT

DRIVING ELEMENT	NAND	AND	NOR	OR	DRIVER	DCL ARRAYS	322 C, R_D, S_D	322 J,K
NAND	12	12	6	6	12	7	4	7
AND	NR	NR	10	10	NR	NR	NR	NR
NOR	5	5	11	11	5	NR	4	7
OR	5	5	11	11	5	NR	4	7
DRIVER	17	17	11	11	17	NR	14	27
DCL ARRAYS	6	NR	NR	NR	NR	10	NR	NR
321 322	5	5	8	8	5	7	4	7
362	5	5	2	2	5	7	4	7

NR = Not Recommended

NOISE MARGIN

DRIVEN ELEMENT

DRIVING ELEMENT		NAND	AND	NOR	OR	DRIVER	DCL ARRAYS
NAND	"0"	400	800	800	800	400	400[1]
	"1"	800	800	800	800	800	1500
AND	"0"	NR	NR	1100	1100	NR	NR
	"1"			900	900		
NOR	"0"	400	800	800	800	400	NR
	"1"	1100	1100	1100	1100	1100	
OR	"0"	400	800	800	800	400	NR
	"1"	1100	1100	1100	1100	1100	
DRIVER	"0"	400	800	800	800	400	NR
	"1"	800	800	800	800	800	
DCL ARRAYS	"0"	600	NR	NR	NR	NR	400
	"1"	700[1]					800
321 322	"0"	400	800	800	800	400	NR
	"1"	1100	1100	1100	1100	1100	

[1] NAND Gate $V0_o$ = 0.4 max at I_{out} = -12.5mA, V_{in} = 2.1 V.

NR = Not Recommended

UTILOGIC II CIRCUITS

UTILOGIC II inputs are classified as sink loads and source loads by the direction of current flow required to activate the input. The input of the OR and NOR gates are called source loads because they must be driven by a source of current, e.g., the output of a UTILOGIC II element in the "1" state or a connection to the positive supply. The inputs of the AND gates, NAND gates and the Binary are called sink loads because they must be driven from a current sink; for example, the output of a UTILOGIC II element in the "0" state or a connection to ground.

In this publication, and all other UTILOGIC II literature, the convention of positive logic, i.e., the positive level is "1", has been assumed. If the negative logic notation is assumed (most negative level is "1"), the AND, OR, NAND and NOR gates become OR, AND, NOR and NAND respectively.

The characteristic curves presented in the various sections are designed to allow the system designer to predict system performance characteristics for various operating conditions. In general, characteristics are normalized to the conditions of the specification sheets. The use of the normalized characteristic is a definite design aid in that it is usually the change in the characteristic as a result of a change in the parameter that is of interest.

As long as the effects, e.g., $\frac{\partial V_{sat}}{\partial Temp.}$, are small, the total effect may be predicted by taking the product of the individual effects.

Throughout the discussion that follows, V_{CC} is assumed to be 5.0V unless otherwise specified.

UTILOGIC II AND Gates

The UTILOGIC II AND gates 305 and 306 are fabricated from the same basic chip, and therefore have identical electrical characteristics. The internal connection pattern is varied to produce a single 6-input AND gate in the 305, and the dual 3-input AND gates in the 306.

CIRCUIT DESCRIPTION

Schematic diagrams of the UTILOGIC II AND gates are shown in Figures 1 and 2. The multiple-emitter input structure provides the same function as a Diode AND gate. The output-emitter follower provides the current gain necessary for high fan-out, and also reduces the offset voltage associated with Diode AND gates. The emitter follower provides a low output impedance to effect fast response on "0" to "1" transitions and the current gain necessary for source current fan-out. The input transistor and connecting diode provide a low impedance circuit to maintain good response on "1" to "0" transitions.

Input Characteristics

The input of the AND is defined as a standard UTILOGIC II sink load. The standard sink load may be simulated by 2 kΩ resistor with a series silicon diode to the supply voltage. The input impedance of UTILOGIC II AND gates

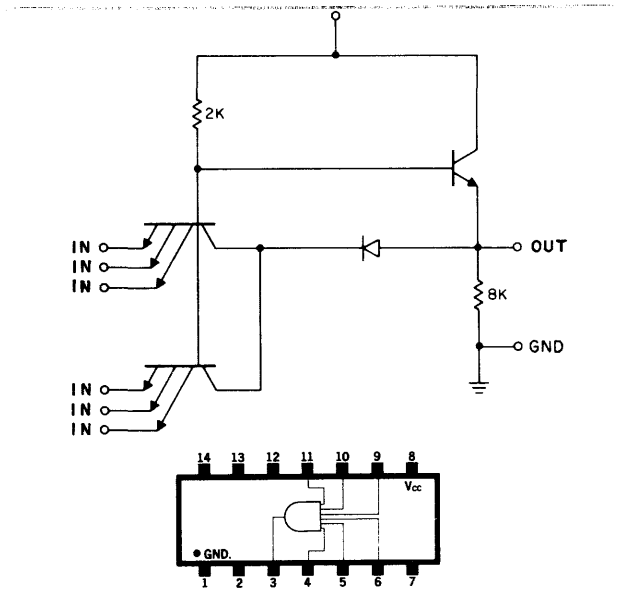


Figure 1 305 6-Input AND Gate

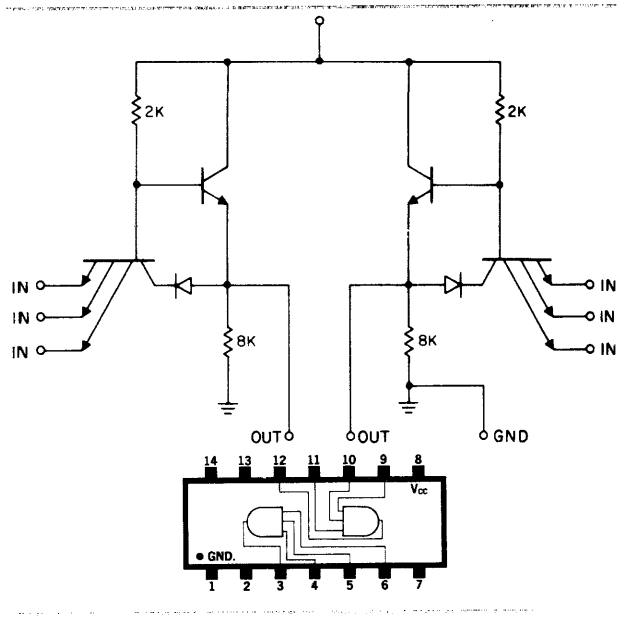


Figure 2 306 Dual 3-Input AND Gate

is low enough so that unused inputs may be left open without degrading circuit performance (open inputs are logical "1") however; it is recommended that unused inputs be connected to the used inputs of the circuit. Connecting the unused inputs to used inputs of the same circuit will not increase the circuit loading. The effect of the added capacitance will be negligible.

Output Characteristics

The fan-out of the UTILOGIC II AND gate is 10 to standard UTILOGIC II source loads. The AND gate does not have output current sinking capability; therefore, it cannot drive sink loads. The AND gate can drive any of the UTILOGIC II source loads. The AND gate outputs should not be paralleled with the outputs of any other circuits as in collector logic configurations. However, outputs of AND gates may be connected to increase fan-out if the inputs of the two circuits are in common.

Characteristic Curves

The following characteristic curves are normalized, when applicable, to the standard data sheet conditions.

Figure 3 shows the test circuit and definition of T_1 and T_2. The switching times (T_1 and T_2) of the UTILOGIC II AND gates are shown as a function of load capacitance, fan-out, supply voltage, temperature, and load resistance.

The input current versus input voltage relationship shown in Figure 4 is vital at interfaces and also allows computation of margins at non-standard conditions of fan-out.

Offset voltage, which is defined as the input voltage minus the output voltage, is shown in Figure 4F as a function of temperature. Full rated load current is applied to the outputs. Input voltages correspond to worst case UTILOGIC II or Binary Element "1" and "0" output voltage levels.

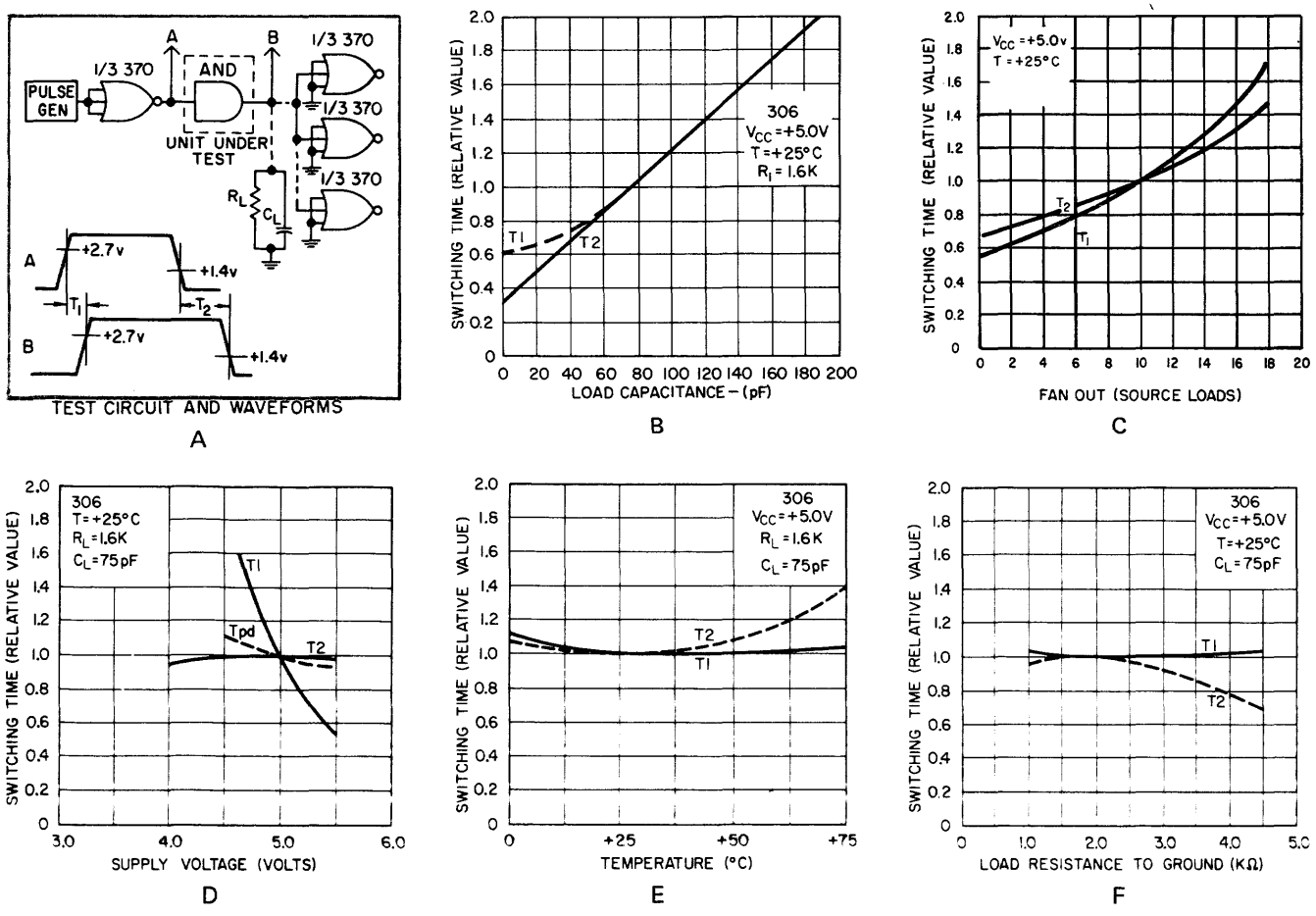


Figure 3 AND Gate Switching Characteristics

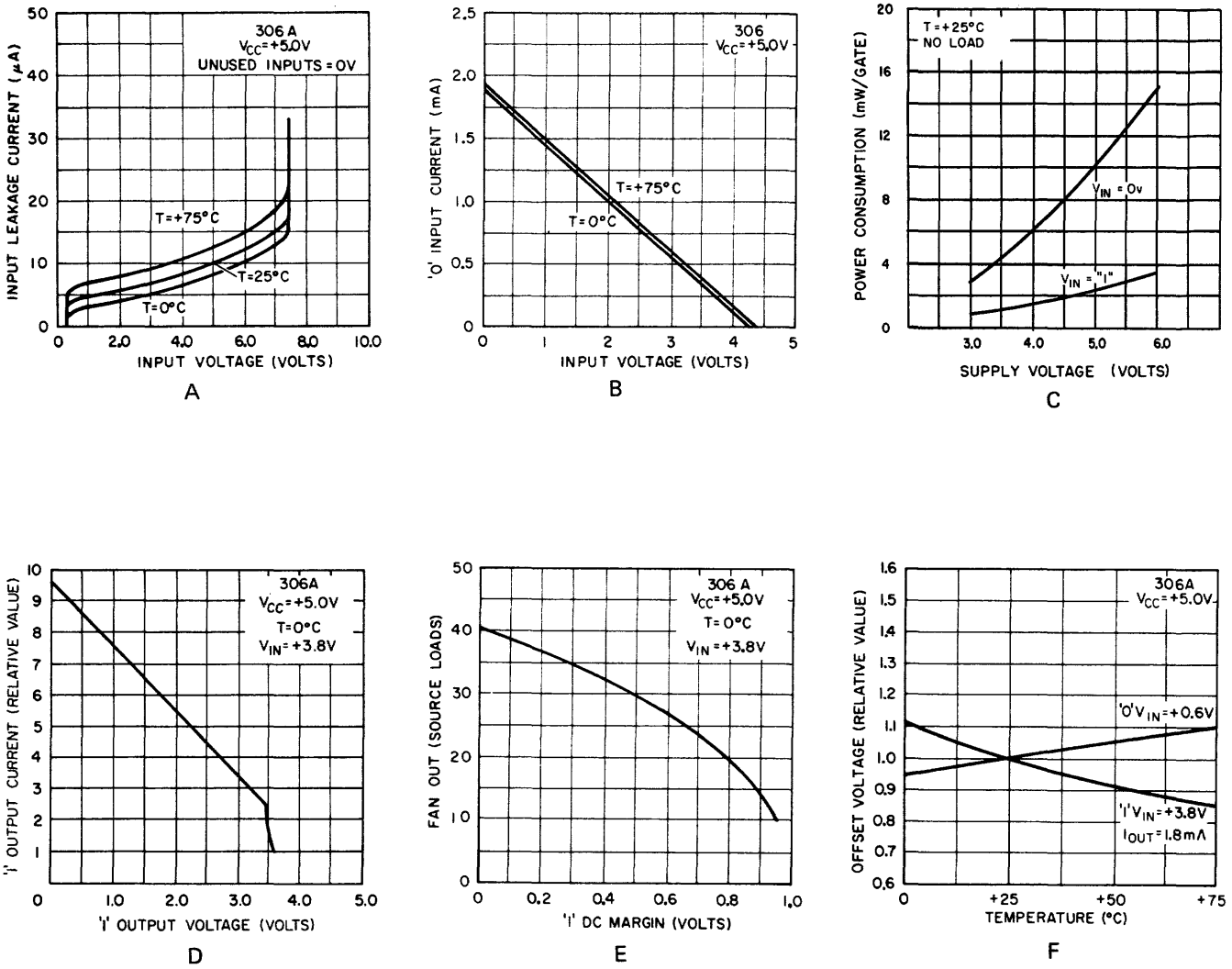


Figure 4 AND Gate DC Characteristics

UTILOGIC II NOR Gates and Expander

The UTILOGIC II NOR gates (314, 370, and 380), Expandable NOR gate (317) and Expander (300), are all derived from the same basic circuit to ensure full compatibility of the Expandable Gates and Expander, and to give all the circuits identical electrical characteristics. However, the 300 and 317 will have longer turn-off delay times (T_2) because of the additional capacitive loading on the expansion input. Turn-on delays (T_1) are not sensitive to this capacitance because the source impedance is low during turn-on.

The 300 Expander circuit is characterized in terms of its operation in conjunction with the 317 Expandable NOR and 333 Expandable OR. The ways in which 300 and 317 (as well as 300 and 333) compatibility is guaranteed are of interest. The expansion forward voltage for the 300 and the expansion input voltage of the 317 are measured under the same conditions, and the same limits are guaranteed. In addition, the 300 input leakage current and the 317 "0" input current specifications guarantee reverse current compatibility. These specifications assure the user that the 300 and 317 or the 300 and 333 combination will have the same DC characteristics as when the 317 or 333 is used alone. AC characteristics are shown later (with the 317 and 333 curves) as a function of the capacitance on the expansion input.

CIRCUIT DESCRIPTION

The UTILOGIC II NOR gate (Figures 5, 6, 7, and 8) may be considered as a derivation of the DTL NOR gate. The input diodes of the DTL NOR were replaced with

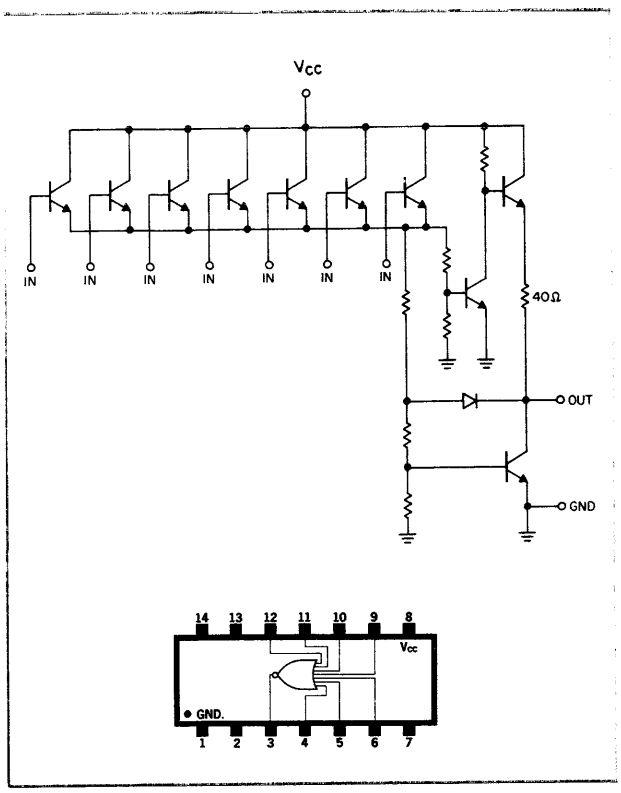


Figure 5 314 7-Input NOR Gate

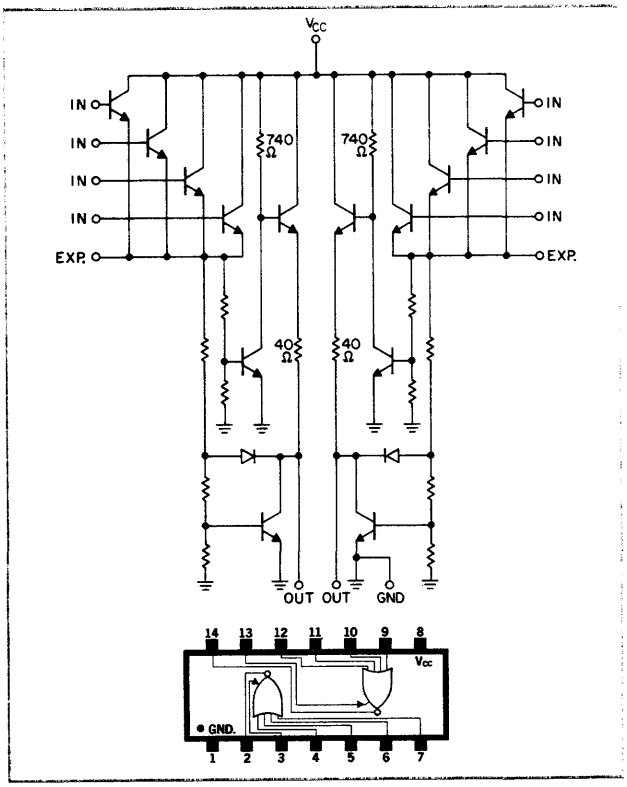


Figure 6 317 Dual 4-Input Expandable NOR Gate

transistors to decrease the input current to allow larger source fan-out capabilities from the NOR and other circuits in the family. The NOR employs a totem-pole output to obtain low output impedance in both the "1" and "0" states. The switching thresholds are determined by the ratio of the coupling resistance to the pull-down resistance at the base of each switching transistor. The series resistor at the output provides current-limiting should the output become accidentally shorted to ground. The Expandable NOR is implemented by connecting the common emitters of the input transistors to an expansion input. The Expander (Figure 9) is a dual array of input transistors; thus, the effect of connecting the Expander output to an expansion input is the same as connecting more input transistors in parallel.

Input Characteristics

The Standard UTILOGIC II Source Load is the NOR input. The Standard Source Load may be simulated by a 15 kΩ resistor and 2 series silicon diodes to ground. An unused NOR input should be tied to ground through a resistance of 60 kΩ (or less) or connected in common with a used input on the same circuit. The capacitance of an open input may become charged during prolonged "1" levels at a driven input. When the driven input goes from "1" to "0", the charged capacitance discharges into the input and gives the effect of a slow circuit. Two or more common inputs represent the same DC load as a single input since the "1" input current is determined by the voltage across the coupling resistors and the gain of the input transistors. Neither of these values changes appreciably when inputs are connected in common. The additional capacitance of a commoned input has no measurable effect on switching times. Input voltages should not exceed the supply voltage unless precautions are taken to limit the resulting current in the collector-base junction of the input transistor to 30 mA.

Output Characteristics

A UTILOGIC II NOR gate has a fan-out of 5 sink loads and 11 source loads. All 16 loads may be connected simultaneously because they do not interact. Because the NOR gates employ transistors for both pull-up and pull-down, their outputs cannot be connected in parallel with the output of any other independent circuit (collector-logic). Parallel operation of an active pull-up device with another device may result in ambiguous output voltages and/or excessively high currents if one device should attempt to reach a "1" level while the other is attempting to reach a level "0". However, two NORs may be connected with common inputs and common outputs. In this case, fan-out is doubled and the input loading is two Standard Source Loads.

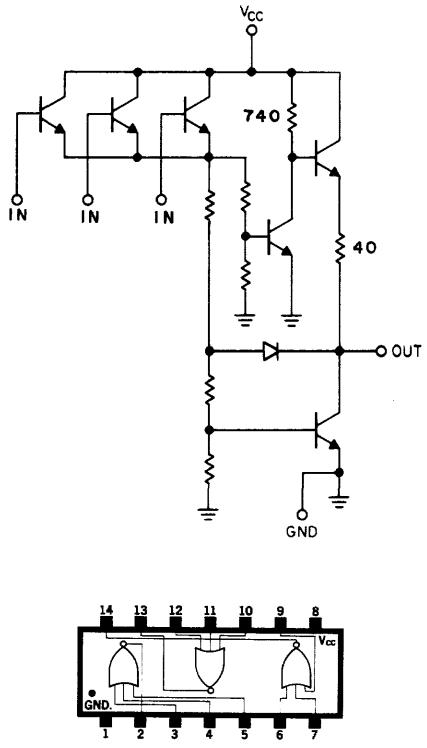
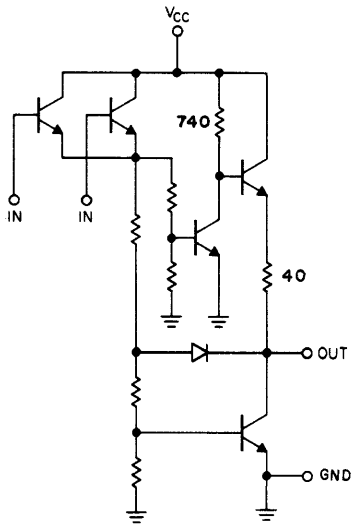


Figure 7 370 Triple 3-Input NOR Gate



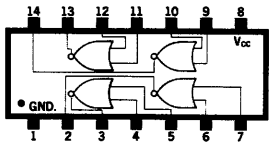


Figure 8 380 Quad 2-Input NOR Gate

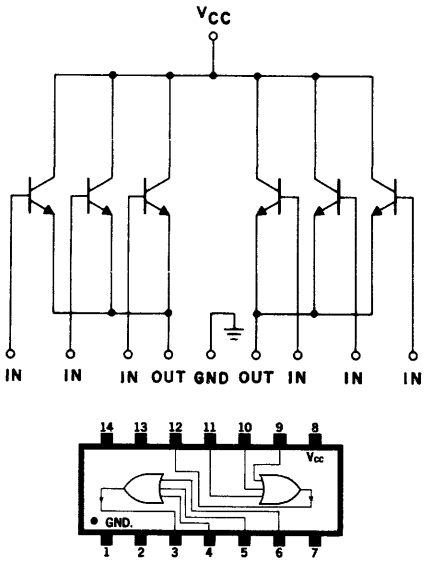
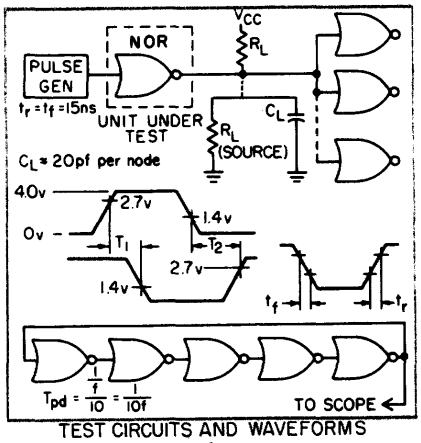
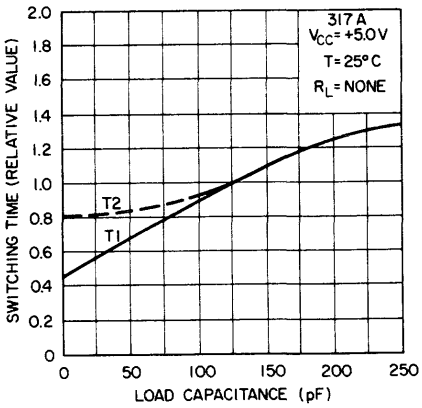


Figure 9 300 Dual 3-Input EXPANDER



TEST CIRCUITS AND WAVEFORMS

A



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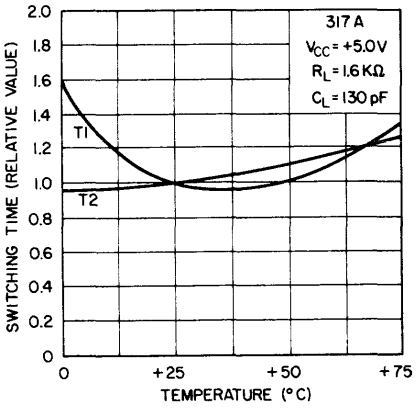
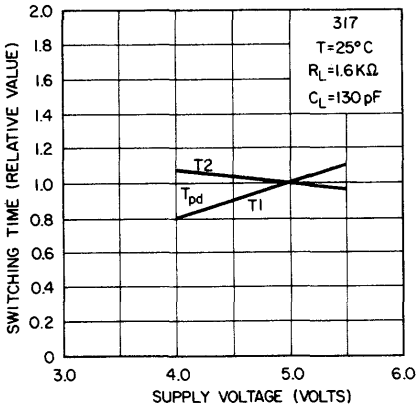
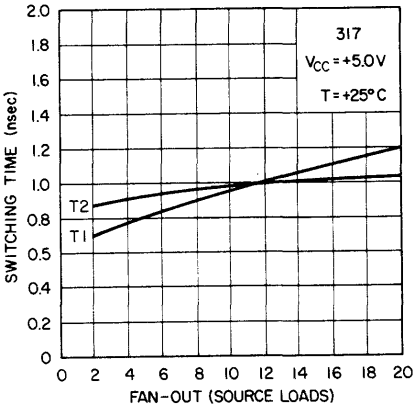


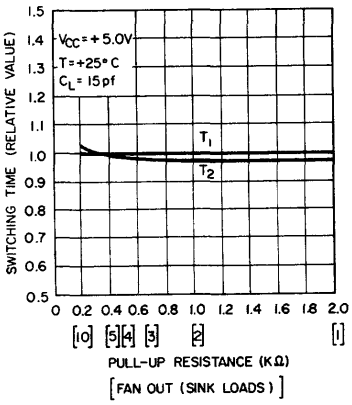
C



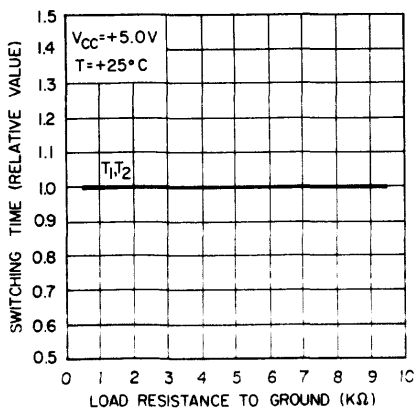
D



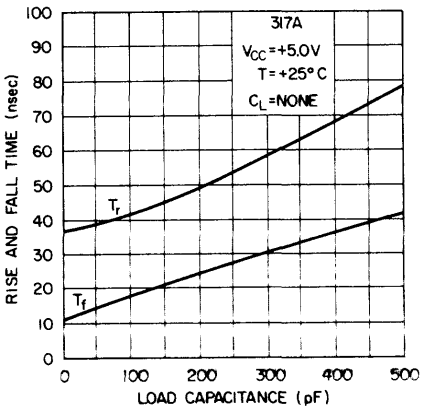
E



F



G



H

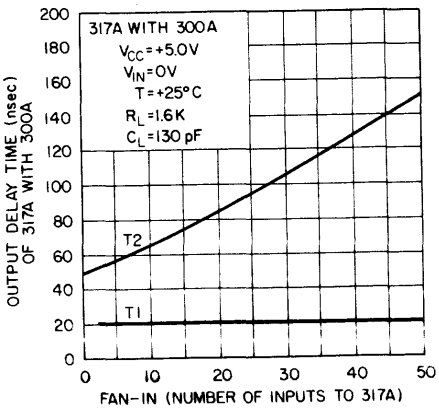


Figure 10 NOR Gate Switching Characteristics

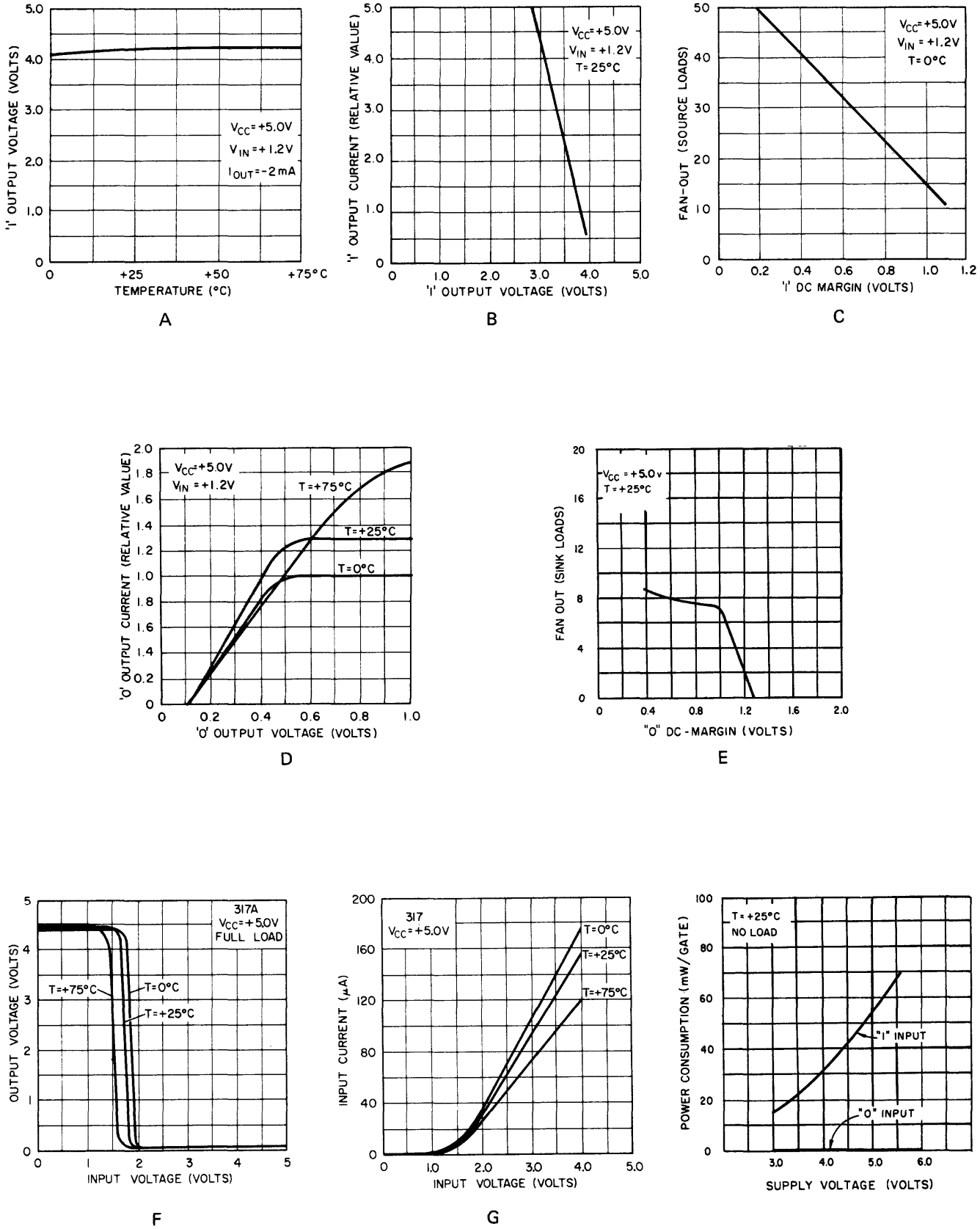


Figure 11 NOR Gate DC Characteristics

UTILOGIC II OR Gates

The UTILOGIC II OR gates are compatible on a pin for pin basis with their UTILOGIC II NOR gate counterparts. This simplifies system design, circuit board layout and checkout.

Comparison of the schematics of the UTILOGIC II OR gate (Figures 13 through 18) and the UTILOGIC II NOR gate (Figures 5, 6, 7, and 8) shows that both types of gates have essentially identical input and output structures; however, the OR gate uses one more transistor to obtain the additional inversion required to produce an OR gate from the basic UTILOGIC II NOR configuration.

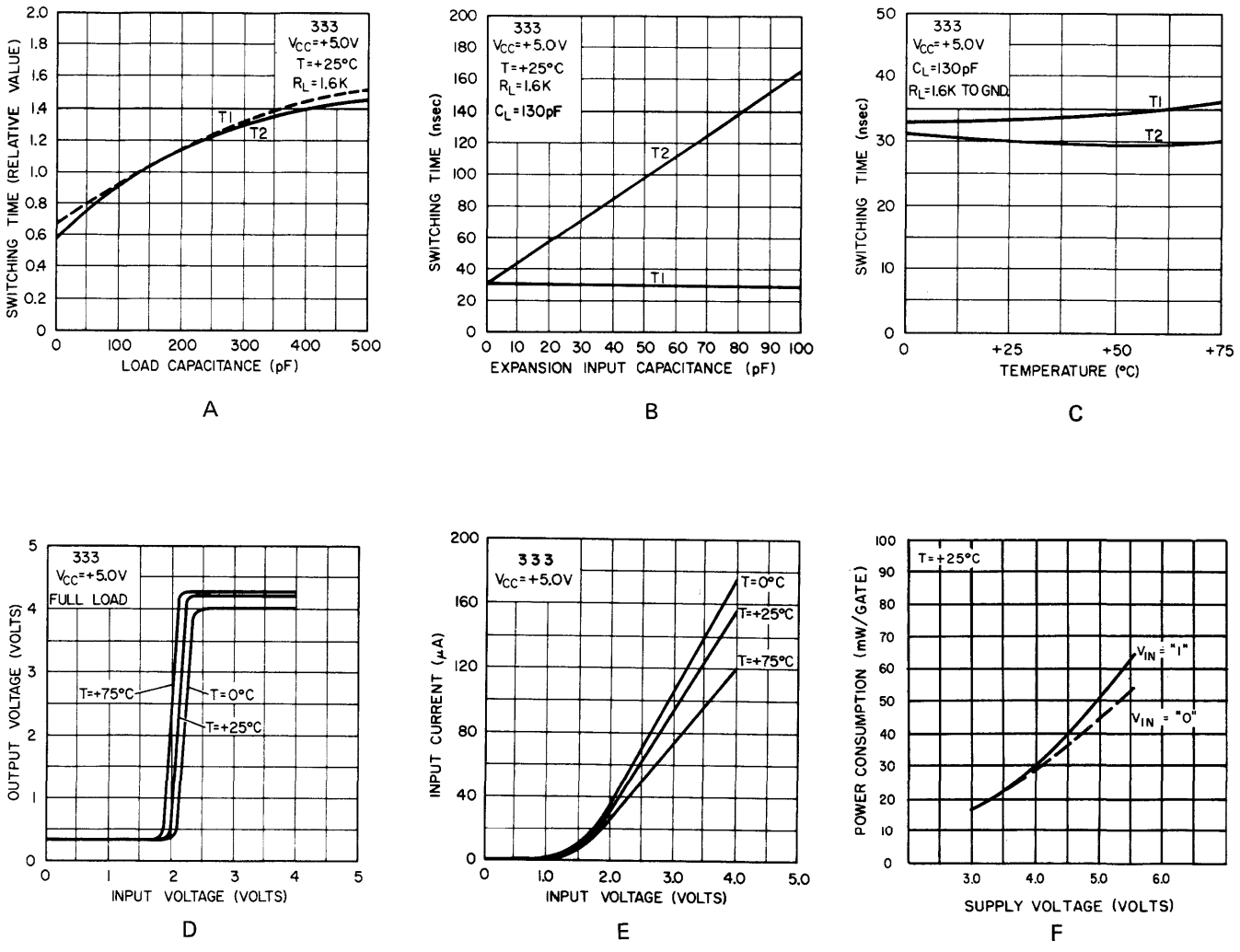


Figure 12 OR Gate Characteristics

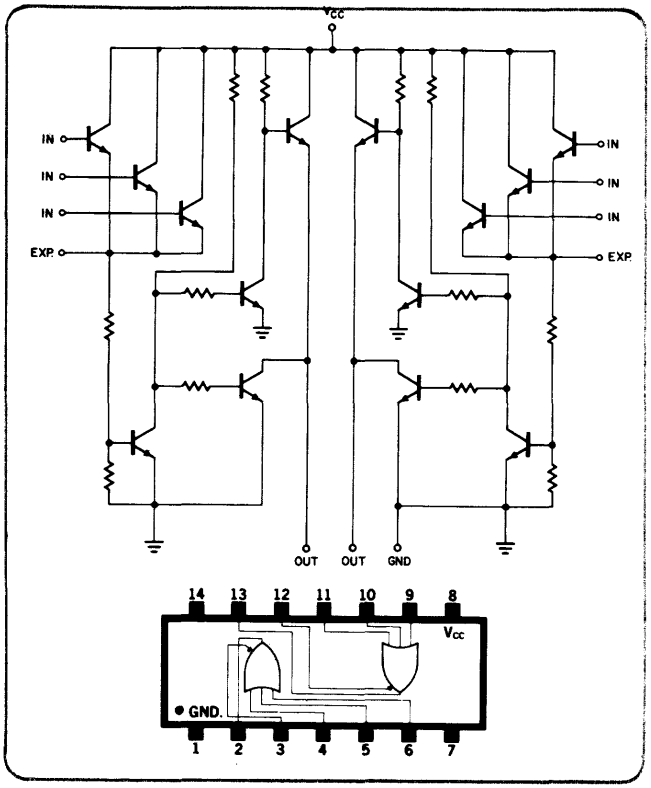


Figure 13 333 Dual 3-Input Expandable OR Gate

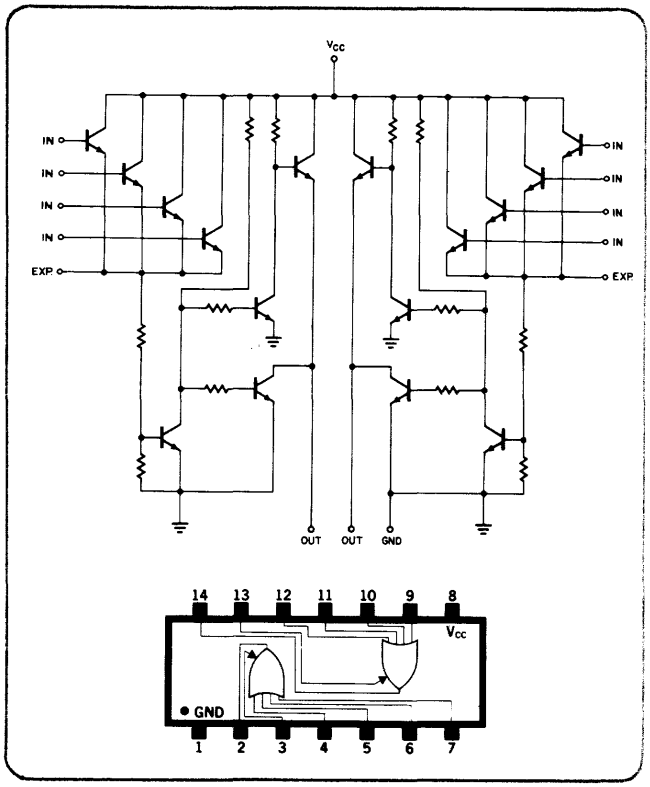


Figure 14 334A Dual 4-Input Expandable OR Gate

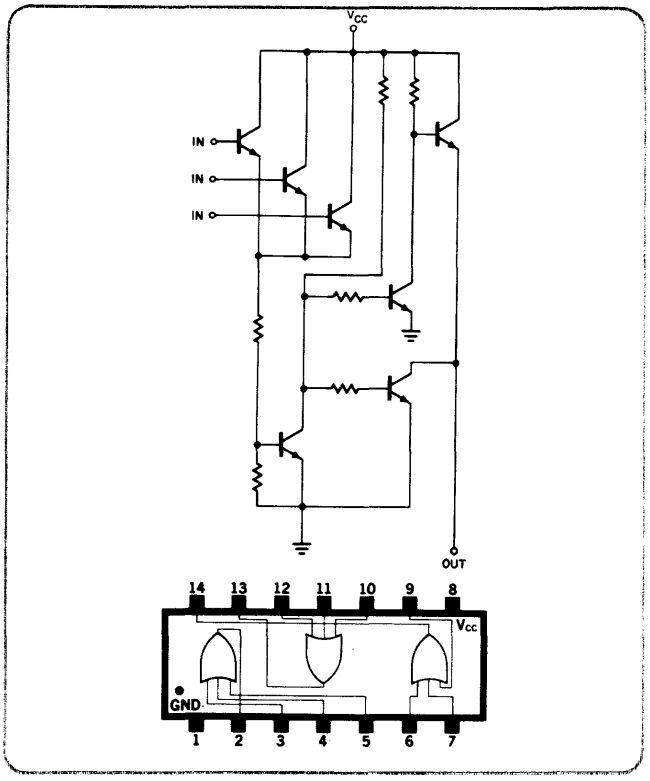


Figure 15 374 Triple 3-Input OR Gate

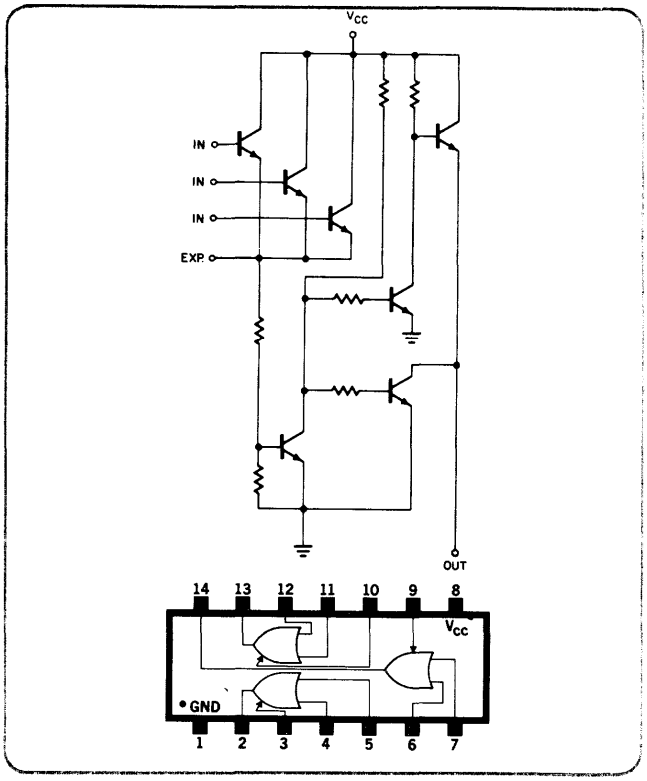


Figure 16 375 Triple 2-Input Expandable OR Gate

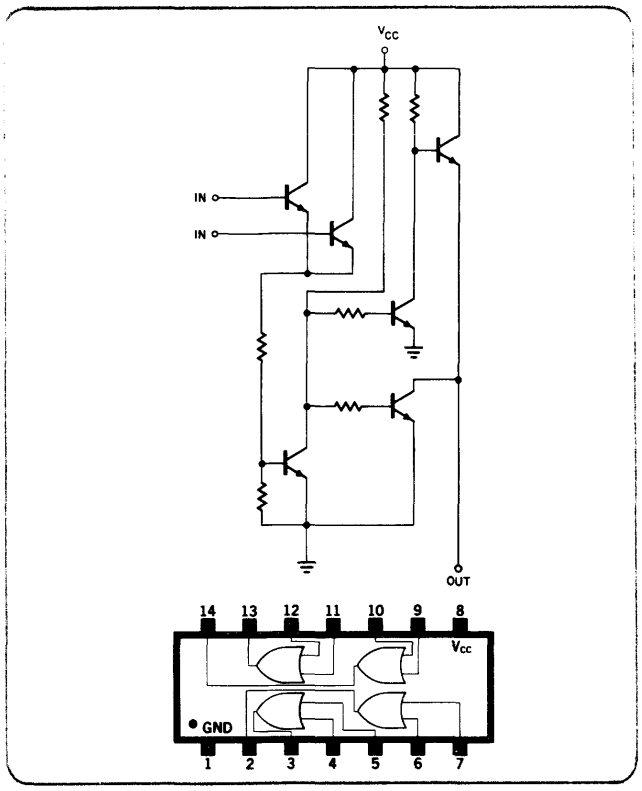


Figure 17 384 Quad 2-Input OR Gate

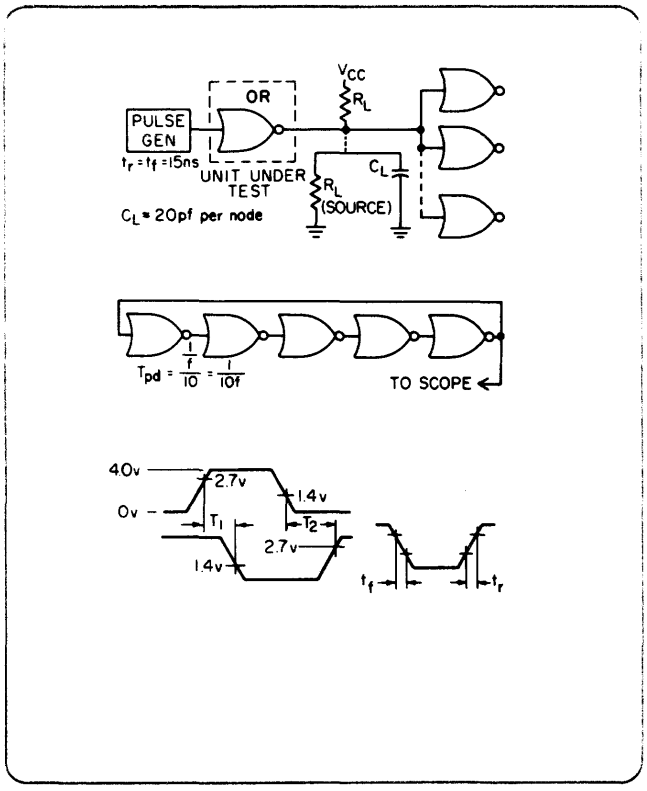


Figure 18 OR Gate Test Circuit and Waveforms

UTILOGIC II NAND Gates and Expander

The UTILOGIC II NAND gates (337, 377 and 387) and diode expander (301) are DTL gates. This is due to the fact that the basic UTILOGIC input structure does not lend itself to implementing the NAND function. The NAND gates are compatible with all other elements in the UTILOGIC II line. In addition, the NAND gates provide a guaranteed interface with Signetics TTL logic elements.

The 301 expander is specified under the same conditions as the gate inputs, thus ensuring that an expanded 337 will have the same input characteristics as the other NAND gates. The 301 may also be used as an expander for the 356 driver element.

CIRCUIT DESCRIPTION

The UTILOGIC II NAND gates (Figures 19, 20, 21, and 22) are modifications of the proven Signetics DTL circuits. The major change is that the usual 4kΩ output resistor has been replaced with a 1kΩ resistor. The use of a passive pull-up permits outputs to be connected in parallel to perform collector logic. Input and output levels are fully compatible with the other UTILOGIC elements and provide a minimum of 800mV of noise margin in both the "0" and "1" states.

Input Characteristics

The input structure of the NAND gates makes them sink loads. The NAND inputs, like the UTILOGIC II AND inputs, require that the driving gate to be able to sink 2.5mA for each such load driven. The UTILOGIC OR and NOR gates can therefore drive up to 5 NAND gate inputs. As with the AND gates, the input load of the NAND gates may be simulated by a 2kΩ resistor in series with a silicon diode to the supply voltage.

Unused inputs may be left open, however, a more conservative design practice suggests connecting the unused inputs to a driven input. In cases where the source load on the driving gate will not permit connecting the unused inputs to a driven input, the unused inputs may be returned to V_{CC}.

The UTILOGIC II NAND gates have two sets of input and output specifications to enable the NAND gates to be used with both UTILOGIC elements and Signetics TTL logic elements. The "1" level input threshold is specified at 2.7 volts for use with UTILOGIC driving elements and 2.1 volts for use with TTL driving elements. This is accomplished by reducing the fan-out at the lower input voltage. The "0" level input current in both cases is within the 2.5mA maximum.

Output Characteristics

A UTILOGIC II NAND gate has a fan-out of 12 sink loads and 6 source loads. All 18 loads may be connected simultaneously. The passive 1kΩ pull-up resistor used in the NAND output structure permits collector logic to be performed by connecting the outputs of up to 5 NAND gates in parallel. The resulting "wired AND" gate can drive one sink load and 6 source loads.

In cases where additional fan-out may be required, NAND gates may be connected in parallel. The fan-out can be doubled by connecting two gates in parallel; however, the input loading is also doubled.

The UTILOGIC II NAND gates can be used to drive Signetics TTL logic elements and complex arrays. When used in conjunction with TTL circuits, the NAND gate sink fan-out is reduced to 12.5mA at a "0" output voltage of 0.4 volts. In most cases, this will result in a fan-out of 7 to Signetics DCL sink type loads. Refer to the Signetics DCL Handbook for further information on DCL input requirements.

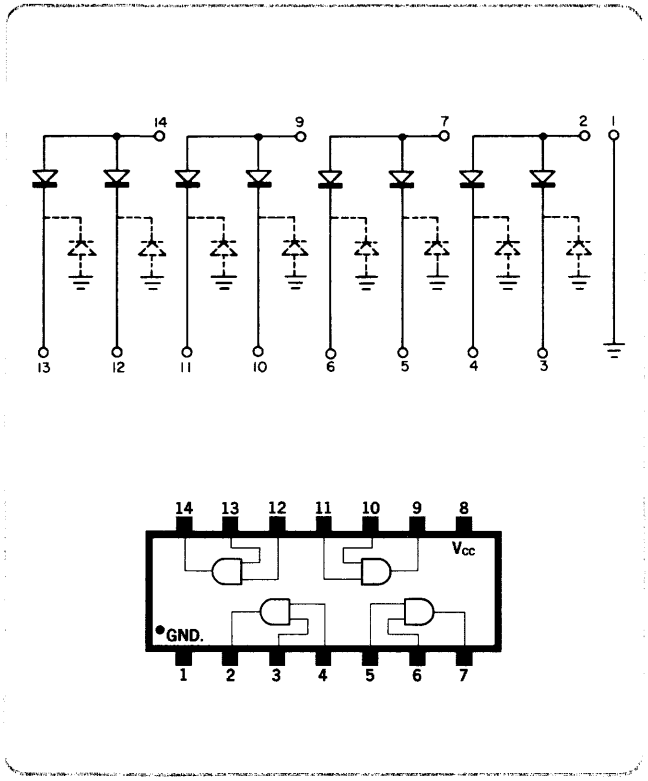


Figure 19 301 Quad 2-Input Gate Expander

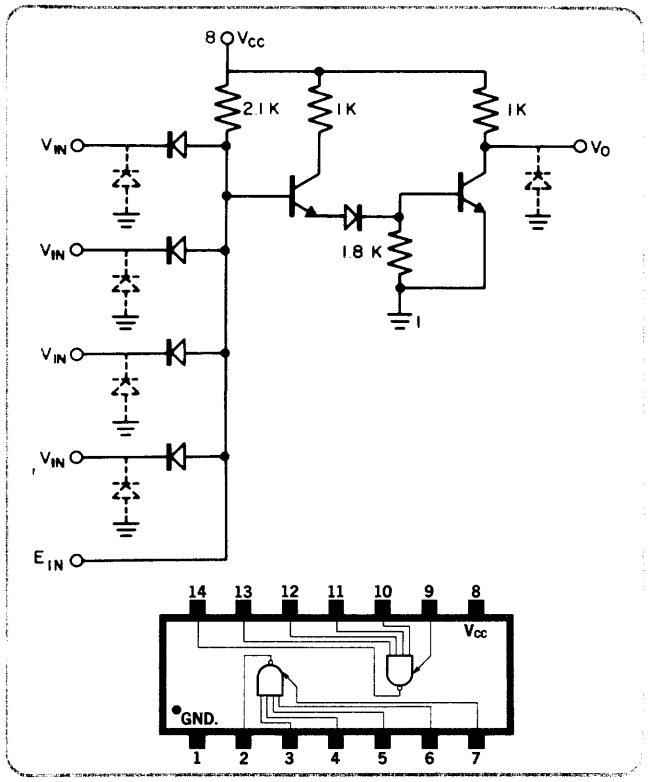


Figure 20 337 Dual 4-Input Expandable NAND Gate

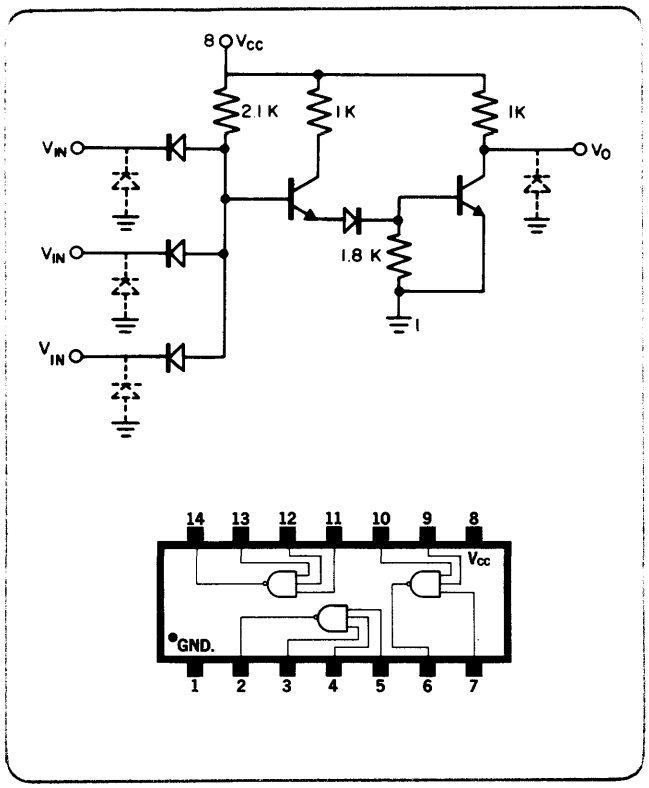


Figure 21 377 Triple 3-Input NAND Gate

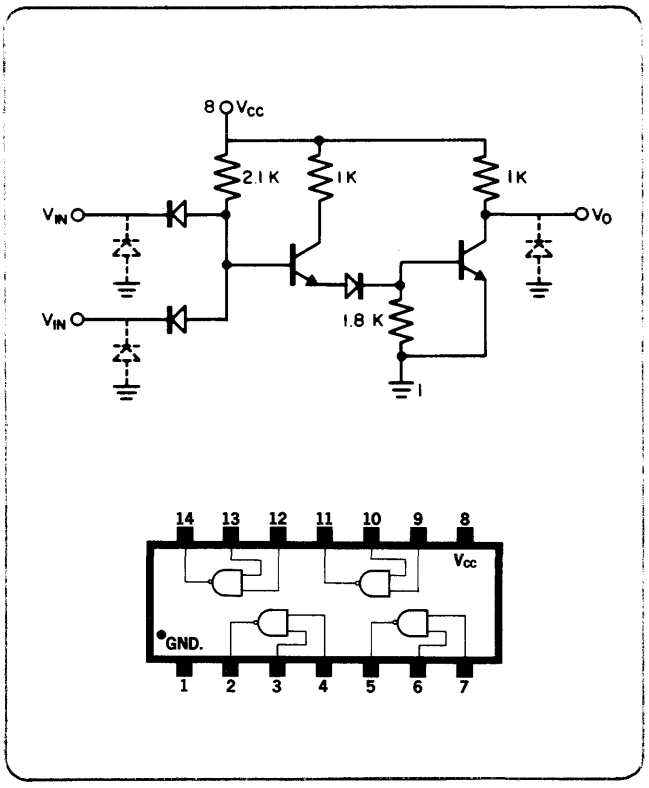


Figure 22 387 Quad 2-Input NAND Gate

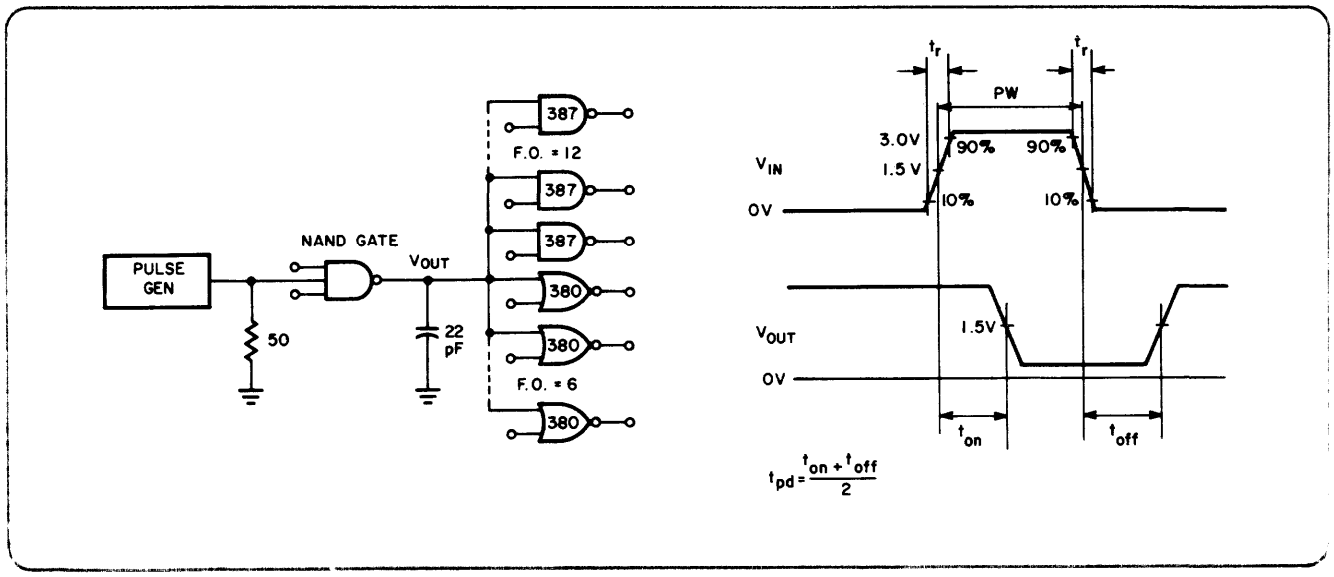


Figure 23 AND Gate Test Circuit and Waveforms